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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,621	12/05/2003	Yang Du	SC13135TC	9075

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,621	DU ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/10/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26-27 are rejected under 35 U.S.C. § 102(a or e) as being anticipated by Cleeves et al. 2003/0139011, newly cited.

Cleeve et al. discloses a method of forming a semiconductor structure, which includes:

providing a substrate 200, fig. 2a+ and para. 30+,

forming a semiconductor fin 208 n+/p-/n+ on the substrate, the fin having first and second sidewalls, see figs. 2e+, para. 33+,

forming a layer of gate material 220 over the substrate 200 and the fin 208 n+/p-/n+, the gate material 220 including a first portion adjacent to the first sidewall of the fin 208 n+/p-/n+ and a second portion adjacent the second sidewall of the fin 208 n+/p-/n+, fig. 2i,

removing the layer of gate material 220 over the semiconductor fin to leave a first gate 224 along the first sidewall and a second gate along the second sidewall, wherein the first and second gates are electrically isolated, fig. 2j-2m and para. 41+,

forming a symmetrical source and drain regions N+ relative to the first and second gates 224 such that a channel region (p- region under gate electrode 224 and between N+ source/drain regions in the fin 208 n+/p-/n+) will be formed under the first and second gates 224 during the operation of the semiconductor structure, fig. 2i-2m and para. 42+, (the also see figs. 1a, 1b, gate electrodes 118-121, source/drain 104/108, channel region 106 and para. 14+)

applying a first signal to the first gate 224, para. 19+,

applying a second signal to the second gate 224,

forming source and drain regions (N+),

source contacts 202 are elelctrical connected (fig. 2q) and drain contacts 226/228 are electrically connected (fig. 2m).

Claims 26 and 28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Voshell et al. 2004/0041189, previously applied.

Voshell et al. discloses a method of forming a semiconductor structure, which includes:

providing a substrate 32, fig. 14 and para.49,

forming a semiconductor fin 33 on the substrate, the fin having first and second sidewalls, see figs. 6-9, para. 36-45,

forming a layer of gate material 44 over the substrate 32 and the fin 33, the gate material 44 including a first portion adjacent to the first sidewall of the fin 33 and a second portion adjacent the second sidewall of the fin 33, see fig. 14,

removing the layer of gate material over the semiconductor fin to leave a first gate along the first sidewall and a second gate along the second sidewall, wherein the first and second gates are electrically isolated,

forming a symmetrical source and drain regions 38, 48 (N+, also see 20/18 of fig. 1, even though the dimension of source and drain are not identical but they are symmetrical relative to the first and second gate electrodes) relative to the first and second gates 44A or 44B such that a channel region (under gate electrode 44A or 44B and between N+ source/drain regions in the pillar 33) will be formed under the first and second gates 44A or 44B during the operation of the semiconductor structure, fig. 10, 14 and para. 38, 39,

applying a first signal to the first gate, para. 49,

applying a second signal to the second gate,

forming source and drain regions (N+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 14-15, 17-20, 22-25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Voshell et al. 2004/0041189.in view of Forbes 6,649,476 and Schulz et al. 2001/0024858.

The reference(s) teach the features:

Voshell et al. '189 discloses a method of forming a semiconductor structure, which includes:

providing a substrate 32 and a semiconductor structure 33 over the substrate 32, the semiconductor structure 33 having a first sidewall, a second sidewall, and a top surface, see figs. 6-9 and para. 36-45,

depositing at least one substantially conformal layer 44 over the substrate, wherein the at least one substantially conformal layer comprises at least a layer of gate material, wherein the at least one substantially conformal layer has a top surface at a height over the semiconductor structure 33, (see para. 38, 47-48. polysilicon layer 44 is disposed on the gate oxide layer 42 and patterned, since, gate oxide 42 formed over the pillar 33, hence, it is clearly polysilicon layer is formed over the pillar and on the gate oxide before patterning),

forming a symmetrical source and drain regions 38, 48 (N+, also see 20/18 of fig. 1, even though the dimension of source and drain are not identical but they are symmetrical relative to the first and second gate electrodes) relative to the first and second gates 44A or 44B such that a channel region (under gate electrode 44A or 44B and between N+ source/drain regions in the pillar 33) will be formed under the first and second gates 44A or 44B during the operation of the semiconductor structure, fig. 10, 14 and para. 38, 39,

forming a substantially planar layer 46A over the substrate below the height of the top surface of the at least one substantially conformal layer over the semiconductor structure 33, see fig. 14 and para.49,

non-abrasively etching through the layer of gate material 44 over the top surface of the semiconductor structure 33,

patterning the at least one substantially conformal layer to form a gate structure 44B prior to the forming the substantially planar layer over the substrate, wherein the non-abrasive etching through the layer of gate material over the top surface of the semiconductor structure 33 further includes etching through the layer of gate material 44 of the gate structure over the top surface of the semiconductor structure 33 to form a first gate portion 44B and a second gate portion 44b that are electrically isolated,

applying a first signal to the first gate 44B, para. 49,

applying a second signal to the second gate 44B,

forming gate contact 44C that is running parallel to the substrate, see fig. 14-15,

forming source and drain regions (n+),

first gate portion are electrically connected together, see fig. 1.

The difference between the reference(s) and the claims are as follows: Voshell et al. teaches applying signals to the first and second vertical gate electrodes but does not teach that the signal is an analog signal. However, Forbes teaches at col. 7, lines 23-67, forming a polysilicon 216 over the silicon pillar 204 then etching to form a polysilicon layer 216 on the sidewall of the silicon pillar 204 and at col. 1, lines 14+ and fig. 11-17, CMOS circuit having first and second vertical gate electrodes 252 can be used in both digital signal (logic) and analog signal. And, analog signal is known in the art as time varying and oscillator signal in known as analog signal. Further more, a preamble is generally not accorded any patentable weight where it merely recites the purpose of a

process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) (process claims, discussed below); Kropa v. Robie,88 USPQ 478, 481 (CCPA 1951)(see MPEP §2111). And, Schulz et al. teaches in figs. 2-3 and para. 45, a silicon nitride film Sd is formed on the first and second vertical gate electrodes

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Voshell et al.'s process by applying analog signals to the first and second vertical gate electrode as suggested by Forbes because the structures can be used both in the logic and analog circuits, such multiplying the signal or video display devices. And, It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Voshell et al.'s process by forming a silicon nitride film on the first and second vertical gate electrode as suggested by Schulz et al. because silicon nitride can be used as etch stop layer during the formation of contact holes.

Claims 13 and 21 and rejected under 35 U.S.C 103 as being unpatentable over Voshell et al. in view of Forbes and Schulz et al. as applied to claims 1-12, 14-15, 17-20, 22-25 above, and further in view of Bissey 2004/0041188.

The difference between the references applied above and the instant claim(s) is: Voshell et al. teaches firming first and second vertical gate transistors but does teaches

connecting all source region together. However, Bissey et al. teaches at fig. 16 that source regions are connected together.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by connecting source region together as taught by Bisssy et al. because a transistor can be operational when source is connected together as common ground electrode. And, power source can be connected between connected drain regions and connected source regions.

Claim 16 is rejected under 35 U.S.C 103 as being unpatentable over Voshell et al. in view of Forbes and Schulz et al. as applied to claims 1-12, 14-15, 17-20, 22-25 above, and further in view of Quek et al. 6,511,884.

The difference between the references applied above and the instant claim(s) is: Voshell et al. teaches firming first and second vertical gate transistors but does teaches ion implanting dopants into the gate material at an angle. However, Quek et al. et al. teaches at fig. 9 and col. 3, lines 60+ that ion implanting dopants into the gate material layer 32.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by ion implanting dopnats into gate layer as taught by Quek et al. because gate electrode can be a conductor.

Claims 27 is rejected under 35 U.S.C 103 as being unpatentable over Voshell et al. as applied to claims 26 and 28 above, and further in view of Bissey 2004/0041188.

The difference between the references applied above and the instant claim(s) is: Voshell et al. teaches firming first and second vertical gate transistors but does teaches connecting all source region together. However, Bissey et al. teaches at fig.16 that source regions are connected together.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by connecting source region together as taught by Bisssy et al. because a transistor can be operational when source is connected together as common ground electrode. And, power source can be connected between connected drain regions and connected source regions.

Claims 28 is rejected under 35 U.S.C 103 as being unpatentable over Cleeves et al. as applied to claims 26 and 27 above, and further in view of Bissey 2004/0041188.

The difference between the references applied above and the instant claim(s) is: Cleeves et al. teaches firming first and second vertical gate transistors but does teaches connecting all gate region together. However, Bissey et al. teaches at fig.1 that gate regions 22 are connected together with WL.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by connecting gate regions together as taught by Bisssy et al. because gate electrode can be used to control the storage charges.

Claims 29 and 30 are rejected under 35 U.S.C 103 as being unpatentable over Cleeves et al. as applied to claims 26 and 27 above, and further in view of Forbes 6,649,476.

The difference between the references applied above and the instant claim(s) is: Cleeves et al. teaches firming first and second vertical gate transistors but does teaches applying analog signal such as oscillator signal to the first and second vertical gate electrodes. However, However, Forbes teaches in col. 1, lines 14+ and fig. 11-17, CMOS circuit having first and second vertical gate electrodes 252 can be used in both digital signal (logic) and analog signal. And, analog signal is known in the art as time varying and oscillator signal in known as analog signal.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Cleeves et al.'s process by applying analog signals to the first and second vertical gate electrode as suggested by Forbes because the structures can be used both in the logic and analog circuits, such multiplying the signal or video display devices.

Claims 29 and 30 are rejected under 35 U.S.C 103 as being unpatentable over Voshell et al. as applied to claims 26 and 28 above, and further in view of Forbes 6,649,476.

The difference between the references applied above and the instant claim(s) is: Voshell et al. teaches firming first and second vertical gate transistors but does teaches applying analog signal such as oscillator signal to the first and second vertical gate

electrodes. However, However, Forbes teaches in col. 1, lines 14+ and fig. 11-17, CMOS circuit having first and second vertical gate electrodes 252 can be used in both digital signal (logic) and analog signal. And, analog signal is known in the art as time varying and oscillator signal in known as analog signal.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Voshell et al.'s process by applying analog signals to the first and second vertical gate electrode as suggested by Forbes because the structures can be used both in the logic and analog circuits, such multiplying the signal or video display devices.

Conclusions

Applicant's arguments filed on Sept.10, 2004 have been fully considered but they are not persuasive. Newly cited reference Cleeves et al. clearly teaches at figs. 1a, 1b, 1c, and para. 14+, forming a symmetrical source and drain regions 104/108 N+ relative to the first and second gates 118-121 such that a channel region 106 (p- region under gate electrode and between N+ source/drain regions) will be formed under the first and second gates 118-121 during the operation of the semiconductor structure, and also at figs. 2i-2m and para. 42+, forming a symmetrical source and drain regions N+ relative to the first and second gates 224 such that a channel region (p- region under gate electrode 224 and between N+ source/drain regions in the fin 208 n+/p-/n+) will be formed under the first and second gates 224 during the operation of the semiconductor structure. And, Voshell also clearly teaches at fig. 10, 14 and para. 38, 39, forming a symmetrical source and drain regions 38, 48 (N+, also see 20/18 of fig. 1, even though the dimension of source and drain are not identical but they are symmetrical relative to

the first and second gate electrodes) relative to the first and second gates 44A or 44B such that a channel region (under gate electrode 44A or 44B and between N+ source/drain regions in the pillar 33) will be formed under the first and second gates 44A or 44B during the operation of the semiconductor structure.

And, Voshell teaches at para. 38, 47-48. polysilicon layer 44 is disposed on the gate oxide layer 42 and patterned, since, gate oxide 42 formed over the pillar 33, hence, it is clearly polysilicon layer is formed over the pillar and on the gate oxide before patterning and Forbes also teaches at col. 7, lines 23-67, forming a polysilicon 216 over the silicon pillar 204 then etching to form a polysilicon layer 216 on the sidewall of the silicon pillar 204. And, Cleeves et al. also clearly teaches at fig. 2i, fig. 2j-2m and para. 41+, forming a layer of gate material 220 over the substrate 200 and the fin 208 n+/p-/n+, the gate material 220 including a first portion adjacent to the first sidewall of the fin 208 n+/p-/n+ and a second portion adjacent the second sidewall of the fin 208 n+/p-/n+, removing the layer of gate material 220 over the semiconductor fin to leave a first gate 224 along the first sidewall and a second gate along the second sidewall.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the customer service whose telephone number is (703) 308-4357 and Fax number (703) 872-9306.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for this Group is (703) 872-9306.

hjt

11/21/04

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800